

REMARKS

The independent claims 1, 5, 16, 30, 37, and 38 are amended to clarify characteristics of the pipelined sub-processes that are part of the recursion process. Support for the amendments may be found in paragraphs [0041] – [0045], and [0049].

The rejections presented in the Office Action dated December 15, 2006, have been considered. Claims 1-38 are pending in the application. Reconsideration and allowance of the application are respectfully requested.

Claims 1-38 are understood to be patentable under 35 USC §103(a) over “Nguyen” (U.S. patent pub. 2003/0097633 to Nguyen) in view of “Van Stralen” (U.S. patent 6,304,996 to Van Stralen et al.). The rejection is respectfully traversed because the Office Action does not show that all the limitations are suggested by the references and does not provide a proper motivation for modifying the teachings of Nguyen with teachings of Van Stralen.

The limitations added to the claims clarify the pipelined sub-processes of the recursion process. For example, in claim 1, each sub-process performs a partial calculation of a probability value output by the recursion process for each sample within the data block. Also, to clarify operation of the pipelined sub-processes, the limitations specify that a first sub-process performs a partial calculation of the probability value for a first sample in a first cycle, a second sub-process performs a partial calculation of the probability value for the first sample in a second cycle that occurs after the first cycle, and the first sub-process performs a partial calculation of the probability value for a second sample in the second cycle. Neither Nguyen nor Van Stralen suggest these limitations.

In Nguyen, each of the MAP decoders 42 and 44 in FIGURE 4 apparently processes an entire window of samples as shown in FIGURE 6 and explained in paragraphs [0054] – [0067]. There is no apparent suggestion that Nguyen’s decoders process the samples in the claimed pipeline manner. As to Van Stralen, the only mention of pipelining is of pipelined trees of summation functions as set forth in Van Stralen’s claim 1. Also, Van Stralen’s alpha and beta recursion circuit of FIG. 8A does not show pipelining of the sub-processes of the recursion process where each pipelined sub-process performs a partial calculation of the probability value as

claimed. Thus, the limitations of claim 1 are not shown to be suggested by the Nguyen-Van Stralen combination.

The asserted motivation for combining Van Stralen's high-speed turbo decoder with Nguyen's high-speed turbo decoder architecture is unsupported by evidence and improper. The asserted motivation states that it would have been obvious to make the combination in order to "provide a turbo decoder which efficiently uses memory and combinatorial logic such that the structure is highly streamlined with parallel signal processing." It is respectfully submitted that there is no evidence presented to support the assertion that Nguyen is does not efficiently use memory, nor is there any evidence presented to support the assertion that Nguyen would benefit from Van Stralen's parallel processing. Therefore, the asserted motivation is improper.

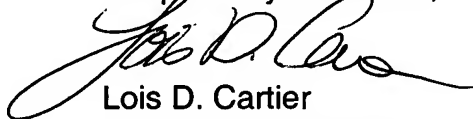
Independent claims 5, 16, 30, 37, and 38 include limitations similar to those of claim 1. Claims 2-4, 6-15, 17-29, and 31-36 depend from the independent claims and further refine the limitations of the independent claims which are discussed above. Therefore, claims 2-38 are also not shown to be unpatentable over the Nguyen-Van Stralen combination.

The rejection of claims 1-38 should be withdrawn because a *prima facie* case of obviousness has not been established.

CONCLUSION

Reconsideration and a notice of allowance are respectfully requested in view of the Remarks presented above. If the Examiner has any questions or concerns, a telephone call to the undersigned is invited.

Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on February 27, 2007.

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